

CLAIMS

- 1 1. A model for representing a bidirectional wire input/output (I/O) during
2 computer simulation of a electronic device, the model comprising:
- 3 a) a first path between a first port and a second port;
- 4 b) a second path between the second port and the first port; and
- 5 c) a control mechanism, the control mechanism checking signal values on the
6 first port and the second port when a change is detected on the first port or the
7 second port, the control mechanism enabling the first path when a change is
8 detected on the first port and the first port does not equal the second port, the
9 control mechanism enabling the second path when a change is detected on the
10 second port and the first port does not equal the second port.
- 1 2. The model of claim 1 wherein the model is implemented in the Verilog
2 hardware description language.
- 1 3. The model of claim 1 wherein the model is implemented in the VHDL
2 hardware description language using Vital timing routines.

1 4. The model of claim 1 wherein the first path comprises a second NMOS device
2 and a fourth NMOS device, and wherein the second path comprises a first
3 NMOS device and a third NMOS device.

1 5. The model of claim 4 wherein the control mechanism enables the first path by
2 enabling the second NMOS device when a change is detected on the first port
3 and the first port does not equal the second port, and wherein the control
4 mechanism enables the second path by enabling the first NMOS device when
5 a change is detected on the second port and the first port does not equal the
6 second port.

1 6. The model of claim 4 wherein the first NMOS device, the second NMOS
2 device, the third NMOS device, and the fourth NMOS device comprise
3 Verilog NMOS primitives.

1 7. The model of claim 4 wherein timing values are annotated in the model and
2 include module input port delays annotated into the third NMOS device and
3 the fourth NMOS device.

1 8. The model of claim 1 wherein timing values are annotated across the first path
2 and the second path.

1 9. The model of claim 8 wherein the timing values are annotated in the form of
2 propagation delays annotated between the first port to the second port and
3 between the second port to the first port.

1 10. The model of claim 1 wherein the control mechanism further disables the
2 second path when a change is detected on the first port and the first port does
3 not equal the second port, and wherein the control mechanism further disables
4 the first path when a change is detected on the second port and the first port
5 does not equal the second port.

1 11. A model for representing a bidirectional wire input/output (I/O) during
2 computer simulation of a electronic device, the model comprising:
3 a) a first path between a first port and a second port, the first path including a
4 second NMOS device,
5 b) a second path between the second port and the first port, the second path
6 including a first NMOS device; and
7 c) a control mechanism, the control mechanism checking signal values on the
8 first port and the second port when a change is detected on the first port or the
9 second port, the control mechanism enabling the second NMOS device when a
10 change is detected on the first port and the first port does not equal the second
11 port, the control mechanism enabling the first NMOS device when a change is
12 detected on the second port and the first port does not equal the second port.

1 12. The model of claim 11 wherein the second path further includes a third
2 NMOS device and wherein the first path further includes a fourth NMOS
3 device, wherein the third and fourth NMOS devices are tied on to function as
4 pass devices.

1 13. The model of claim 12 wherein the timing values are annotated into the model
2 in the form of module input port delays annotated into the third NMOS device
3 and the fourth NMOS device.

1 14. The model of claim 11 wherein the timing values are annotated into the model
2 in the form of propagation delays across the first path and the second path.

1 15. The model of claim 11 wherein the first and second NMOS devices comprise
2 Verilog NMOS primitives.

1 16. The model of claim 11 wherein the control mechanism further disables the
2 first NMOS device when a change is detected on the first port and the first
3 port does not equal the second port, and wherein the control mechanism
4 further disables second NMOS device when a change is detected on the
5 second port and the first port does not equal the second port.

1 17. A method for representing a bidirectional wire input/output (I/O) during
2 computer simulation of an electronic device, the method comprising:
3 a) providing a model for the bidirectional wire I/O, the model including:
4 i) a first path between a first port and a second port; and
5 ii) a second path between the second port and the first port;
6 b) checking signal values on the first port and the second port when a change
7 is detected on the first port or the second port;
8 c) enabling the first path when a change is detected on the first port and the
9 first port does not equal the second port;
10 d) enabling the second path when a change is detected on the second port and
18 the first port does not equal the second port.

1 18. The method of claim 17 further comprising the steps of:
2 e) disabling the second path when a change is detected on the first port and the
3 first port does not equal the second port;
4 f) disabling the first path when a change is detected on the second port and the
5 first port does not equal the second port.

1 19. The method of claim 17 further comprising the step of annotating timing
2 values across the first path and the second path.

1 20. The method of claim 17 wherein the model further includes a wherein a
2 second NMOS device and a fourth NMOS device in the first path and further
3 includes a first NMOS device and a third NMOS device in the second path.

1 21. The method of claim 20 further comprising the step of annotating module
2 input port delays into the third NMOS device and the fourth NMOS device.

- 1 22. A program product comprising:
- 2 A) a hardware description language model for representing a bidirectional
- 3 wire input/output (I/O) during computer simulation of a electronic device, the
- 4 hardware description language model including:
- 5 i) a first path between a first port and a second port;
- 6 ii) a second path between the second port and the first port; and
- 7 iii) a control mechanism, the control mechanism checking signal
- 8 values on the first port and the second port when a change is detected
- 9 on the first port or the second port, the control mechanism enabling the
- 10 first path when a change is detected on the first port and the first port
- 11 does not equal the second port, the control mechanism enabling the
- 12 second path when a change is detected on the second port and the first
- 13 port does not equal the second port;
- 14 B) signal bearing media bearing the hardware description language model.
- 1 23. The program product of 22 wherein the signal bearing media comprises
- 2 transmission media.
- 1 24. The program product of 22 wherein the signal bearing media comprises
- 2 recordable media.

1 25. The program product of claim 22 wherein the model is implemented in the
2 Verilog hardware description language.

1 26. The program product of claim 22 wherein the model is implemented in the
2 VHDL hardware description language using Vital timing routines.

1 27. The program product of claim 22 wherein the first path comprises a second
2 NMOS device and a fourth NMOS device, and wherein the second path
3 comprises a first NMOS device and a third NMOS device.

1 28. The program product of claim 27 wherein the control mechanism enables the
2 first path by enabling the second NMOS device when a change is detected on
3 the first port and the first port does not equal the second port, and wherein the
4 control mechanism enables the second path by enabling the first NMOS
5 device when a change is detected on the second port and the first port does not
6 equal the second port.

1 29. The program product of claim 27 wherein the first NMOS device, the second
2 NMOS device, the third NMOS device, and the fourth NMOS device
3 comprise Verilog NMOS primitives.

1 30. The program product of claim 27 wherein timing values are annotated into the
2 model that include module input port delays annotated into the third NMOS
3 device and the fourth NMOS device.

1 31. The program product of claim 22 wherein timing values are annotated across
2 the first path and the second path.

1 32. The program product of claim 31 wherein the timing values are annotated in
2 the form of propagation delays annotated between the first port to the second
3 port and between the second port to the first port.

1 33. The program product of claim 22 wherein the control mechanism further
2 disables the second path when a change is detected on the first port and the
3 first port does not equal the second port, and wherein the control mechanism
4 further disables the first path when a change is detected on the second port and
5 the first port does not equal the second port.
